A 5V to 3.3V, 7A, Synchronous Rectified Buck Regulator Using the Intersil SynchroFET™ HIP5011

Application Note | September 1995 | AN9526

Introduction

The Intersil SynchroFET is a new approach in partitioning a synchronous rectified buck regulator. The device combines power MOSFETs and drive circuitry to enable synchronous rectification beyond 1MHz. Integrating the drive circuitry and power MOSFETS in one silicon device offers numerous advantages. These include increased frequency operation, lower gate-charge, parasitic component reduction, precise control of MOSFET switching via adaptive “shoot-through” protection and elimination of the external Schottky rectifier associated with a discrete solution. In addition, the tab of the SynchroFET is tied to the substrate. This enables grounding of the tab for greater thermal performance and lower EMI. The device also operates in the continuous conduction mode independent of load current. This results in a stable loop response from no-load to full-load. A smaller inductor size is attained with continuous conduction since the circuit will never enter the discontinuous mode. What’s more, discontinuous mode ringing at light loads is eliminated further reducing EMI. To fully realize the ripple voltage specification, the maximum allowable ripple current is bounded by the equivalent series resistance (ESR) of the output capacitance not the output inductance value. This causes the inductor to be much smaller than in the standard buck regulator. Furthermore, the SynchroFET can be driven with a simple low cost voltage or current mode controller. This eliminates costly application specific controller interfacing.

The SynchroFET is ideal for implementing 5V to ≤3.3V or 3.3V to ≤2.9V converters. Efficiencies greater than 90% are easily implemented, while achieving output powers in the 20W range. There are two versions of the SynchroFET. The HIP5010 has a non-inverting PWM input and can be used with controllers that drive single-ended N-Channel MOSFETS. The HIP5011 has a inverting PWM input and can be used with controllers that drive single-ended P-Channel MOSFETs.

HIP5011EVAL Board

The schematic for the HIP5011EVAL board is shown in Figure 1. The circuit operates at a constant frequency of 400kHz. It accepts a 5V input and delivers a 3.3V output at 7ADC. The 12V supply provides bias power to the HIP5011 and powers the controller. As the schematic shows, the HIP5011 can be interfaced with a very low cost controller. In fact, this particular controller from Texas Instruments has no MOSFET drivers making it low cost and a great companion to the HIP5011. The board was designed to accept a surface mount heat sink (Wakefield Engineering #216 series). However, there is enough copper area on the evaluation board where the heatsink is not necessary. Although, noticeable improvement can be observed using the heatsink within a path of airflow. The design process to follow will be demonstrated for the 3.3V, 7A, HIP5011EVAL board operating in a 25°C environment.

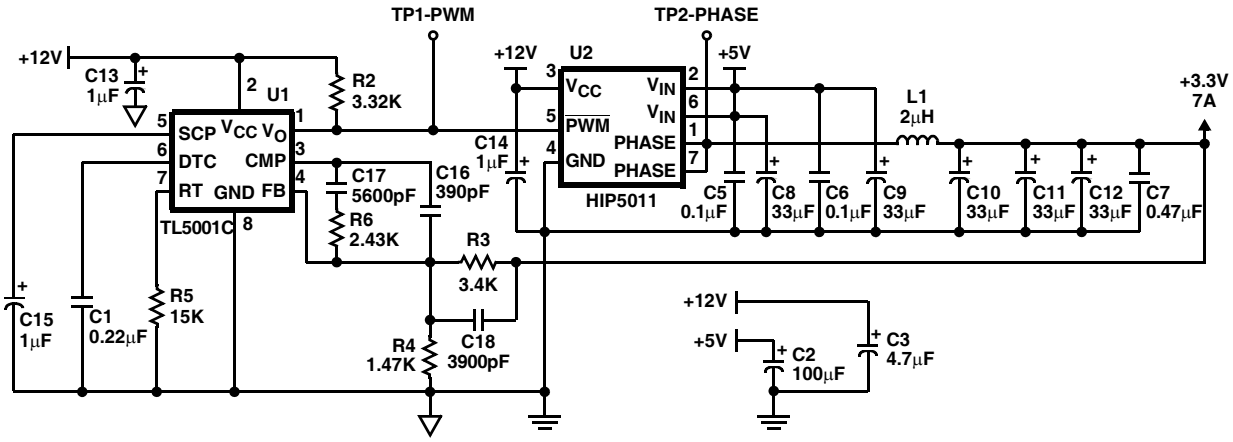

FIGURE 1. SynchroFET DEMO-BOARD SCHEMATIC

Designing the Output Filter

To determine the output inductor value, the duty cycle and input current must be calculated. There are three resistive elements within the SynchroFET circuit model shown in Figure 2. From this model the equation for duty cycle is as follows:

$$D = \frac{V_O + I_{LOAD}(R_W + R_{DSL})}{V_{IN} + I_{LOAD}(R_{DSL} - R_{DSU})} \quad \text{(EQ. 1)}$$

D = Duty Cycle

V_O = Output Voltage

V_{IN} = Input Voltage

I_{LOAD} = Load Current

R_W = Inductor Winding Resistance

R_{DSU} = $r_{DS(ON)}$ of the Upper MOSFET

R_{DSL} = $r_{DS(ON)}$ of the Lower MOSFET

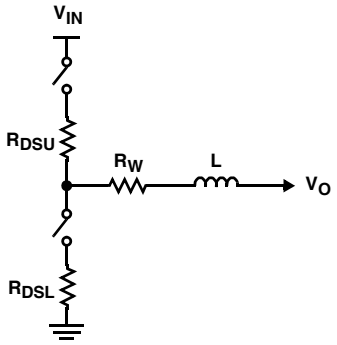

FIGURE 2.

The following parameters are known:

V_O = 3.3V

V_{IN} = 5V

V_{INMAX} = 5.25V

I_{LOAD} = 7A

R_{DSU} = 0.065Ω

R_{DSL} = 0.068Ω

Assume that the winding resistance of the inductor is zero since it is unknown at this time. Later this value can be determined and the inductance can be recalculated.

The unknown parameters are:

R_W = 0Ω

ΔI = Ripple Current

I_{IN} = RMS Input Current

The RMS input current can be calculated by using the following equation:

$$I_{IN} = D \bullet \sqrt{\frac{\left(I_{LOAD} - \frac{\Delta I}{2}\right)^2 + \left(I_{LOAD} - \frac{\Delta I}{2}\right) \bullet \left(I_{LOAD} + \frac{\Delta I}{2}\right) + \left(I_{LOAD} + \frac{\Delta I}{2}\right)^2}{3}} \quad \text{(EQ. 2)}$$

Before calculating the output inductance value, acceptable ripple current needs to be determined. As stated earlier, to fully realize the ripple voltage specification, the maximum allowable ripple current is bounded by the ESR of the output capacitance. In other words, the ESR of the output capacitance sets the maximum ripple current allowable to meet the ripple voltage specification. This is quite different from a standard buck regulator. In a standard buck, the ripple current is limited by the boundary between continuous and discontinuous mode operation. The result of this boundary condition can cause the inductor to be large, especially if the minimum load requirement is low. In the synchronous rectified buck regulator, the converter is always running in the continuous mode. Even at no load! Therefore the ripple current can be made much larger, limited only by the output capacitance ESR value which ultimately sets the ripple voltage specification.

Choosing a ripple current equal to 20% of the rated output current results in 1.4A of ripple current. For 10mV of ripple voltage the minimum output capacitance and maximum ESR requirements are:

$$C_{MIN} = \frac{\Delta I_O}{8 \bullet F_S \bullet \Delta V_O} \quad \text{(EQ. 3)}$$

$$C_{MIN} = \frac{1.4}{8 \bullet 400000 \bullet 0.01} = 44\mu F$$

$$ESR = \frac{\Delta V_O}{\Delta I_O} = \frac{0.01}{1.4} = 0.007\Omega$$

A polymer aluminum capacitor made by Panasonic and Cornell Dubilier has very low ESR values. Their 33µF capacitors have an ESR of 0.015Ω at a switching frequency of 400kHz. Three of these 33µF capacitors in parallel will yield 0.005Ω, meeting the requirements listed above.

The inductor can now be calculated keeping in mind that the maximum ripple current occurs at the maximum input voltage:

$$L = \frac{(V_{INMAX} - V_{DROP} - V_O) \bullet D \bullet t}{\Delta I_O} \quad \text{(EQ. 4)}$$

$$D = \frac{3.3 + 7 \bullet (0 + 0.068)}{5.25 + 7 \bullet (0.068 - 0.065)} = 0.716$$

$$I_{IN} = \left(0.716 \bullet \sqrt{\frac{(7 - 0.7)^2 + 7 - 0.7 \bullet (7 + 0.7) + (7 + 0.7)^2}{3}}\right) = 5.02A$$

$$V_{DROP} = I_{IN} \bullet (R_{DSU} + R_W)$$

$$V_{DROP} = 5.02 \bullet (0.065 + 0) = 0.326V$$

$$L = \frac{(5.25 - 0.326 - 3.3) \bullet 0.716 \bullet 2.5 \bullet 10^{-6}}{1.4} = 2.08\mu H$$

From this calculation a 2µH inductor was chosen from Coiltronics CTX2-4. This particular inductor has a DC winding resistance of 0.008Ω. Running through the previous equations with this winding resistance yields the following:

$D = 0.727$

$I_{IN} = 5.1A$

$V_{DROP} = 0.372V$

$L = 2.05\mu H$

Control Loop Stabilization

The output capacitance and ESR combination of C10, C11 and C12 results in the ESR zero being pushed out to 318kHz, making it unable to aide in loop stability. As a result, a type-three compensation loop was implemented. The unity gain crossover was chosen to be 1/10th the switching frequency or 40kHz. Detailed implementation of control-loop design and component synthesis is beyond the scope of this text. However, references [3] and [5] do address this topic further. Basic concepts covered here will enable proper modeling and verification of the loop response. The loop was simulated using Cadence's Analog Workbench, however any SPICE based modeling program can be used. The model used is shown in Figure 3.

Modeling the Error Amplifier

The parameters for the error amplifier are given in the TL5001 data sheet. The first gain stage of the error amplifier model is the open-loop gain stage A_{VOL}. This is followed by an RC network providing a one pole roll-off, yielding a unity gain crossover of 1.5MHz. This is the minimum specified bandwidth for the error amplifier. The next stage is a buffer followed by the amplifiers output impedance. This completes the model of the controller error amplifier.

Modeling the Power Stage

The power stage begins with the pulse-width modulator gain A_{PWM}. This gain comes from the compensation voltage varying the duty cycle, which ultimately controls the output voltage. Referencing the TL5001 data sheet, a graph depicts compensation voltage variation at 400kHz. It is seen that the compensation voltage variation is from 0.5V (0% duty cycle) to 1.5V (100% duty cycle). The PWM gain is:

$$G_{PWM} = \frac{\Delta V_O}{\Delta V_{OCOMP}} = \frac{5 - 0}{1.5 - 0.5} = 5 = 14dB \quad \text{(EQ. 5)}$$

The remainder of the power stage simulation denotes the SynchroFET $r_{DS(ON)}$ resistance, LC output filter with associated inductor winding resistance, capacitance ESR and full-load resistance.

Figure 4 shows the three separate curves. This top curve is the open-loop response of the TL5001 error amplifier. Notice that the unity gain crossover is 1.5MHz as specified in the data sheet. The middle curve shows the LC filter gain response which begins at 14dB due to the modulator gain. The LC filter has a break frequency of 11kHz. The bottom curve is the output filter phase response. The phase attempts to traverse 180 degrees but is stymied by the ESR zero at 318kHz.

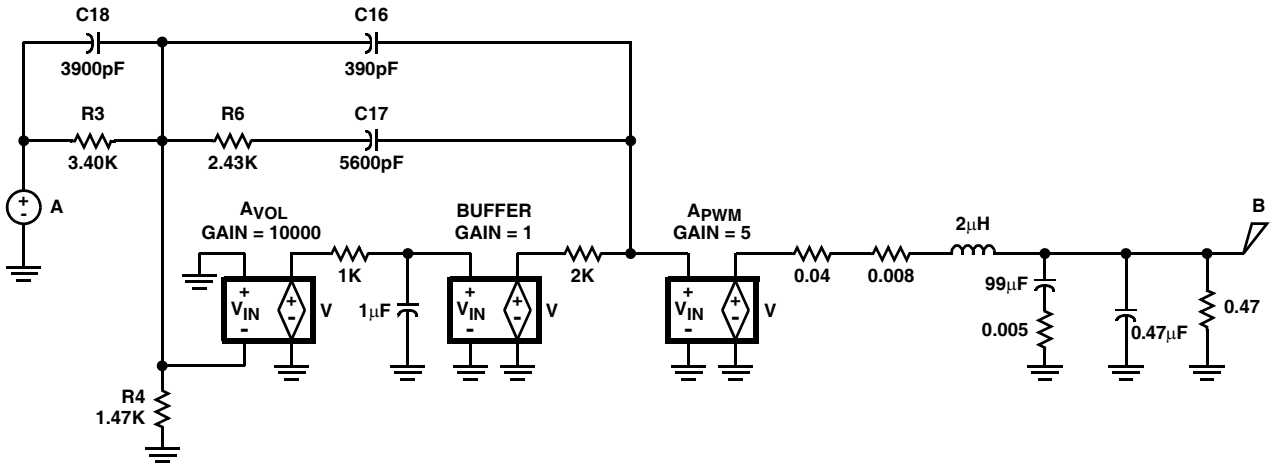

FIGURE 3. HIP5011 CONTROL LOOP MODEL USING THE TL5001 CONTROLLER

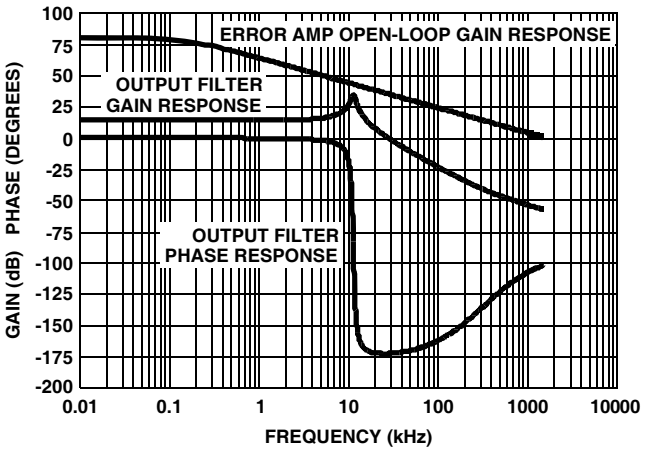

FIGURE 4.

Modeling the Compensation Network

The schematic representation of the type-three compensation network is shown in Figure 5. R3 and R4 set the output voltage. Type three compensation components are shown about the error amplifier model in Figure 3.

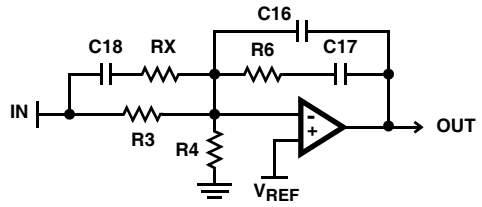

FIGURE 5.

This compensation scheme has two zeros and two poles and is used when ESR values are too low to aide in the loop stability, the case we have here. The two zeros of the compensation loop cancel the two poles of the LC output filter, while the two poles yield sufficient roll-off at higher frequencies. The response of the compensation loop is shown in Figure 6 showing two zeros located at 11kHz and two poles at 160kHz. Also shown in Figure 6 is the open loop gain response of the error amplifier.

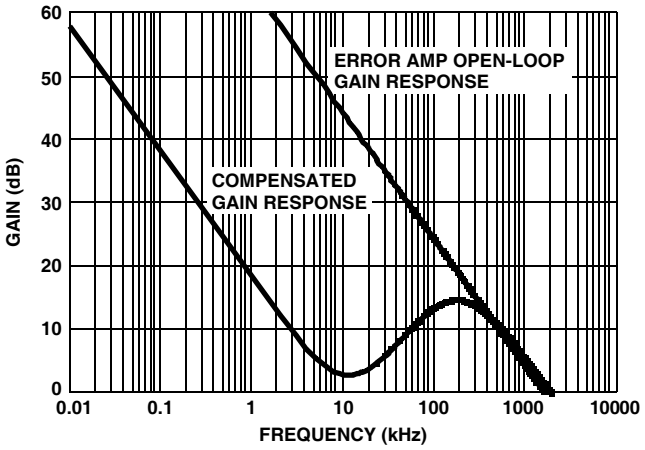

FIGURE 6.

Finally, the combination of the compensation loop response with the power train response yields the results shown in Figure 7. Here is a stable overall loop response with a unity gain crossover at 40kHz and a phase margin of nearly 45 degrees before the phase traverses 360 degrees.

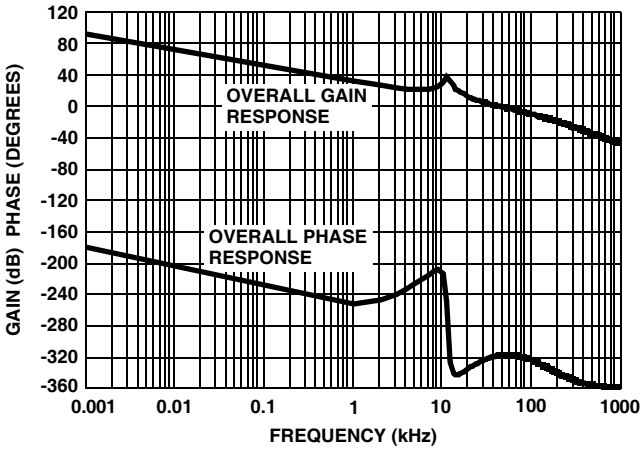

FIGURE 7.

One final note. In the actual HIP5011EVAL board resistor RX was removed from the compensation network of Figure 5, because in this case, it is somewhat superfluous. This removes one of the poles in the transfer-function. This does not present a problem since the natural roll-off response of the error amplifier will aide the attenuation of the upper frequencies. This is exemplified in Figure 6.

HIP5011 Power Loss Analysis

Before getting into the details of the power loss analysis, the HIP5011EVAL board was characterized for thermal resistance. It was determined that with the amount of copper on the board and the SynchroFET surface mounted to that copper, the thermal resistance from junction to ambient was approximately:

$$\theta_{JA} = 30^{o}C/W$$

It was also determined that the SynchroFET case could be kept below 110^{o}C at full load with a room temperature of 22^{o}C. Therefore we can determine the total power dissipated in the SynchroFET as:

$$P_T = \frac{T_J - T_A}{\theta_{JA}} = \frac{110 - 22}{30} = 2.93W$$

This total power dissipation within the SynchroFET culminates from three sources. These are:

- Gate Drive Power Losses
- Switching Losses
- Conduction Losses

Gate Drive Power Losses: The gate drive power losses result in the power dissipated within the gate drivers. This power is a result of displacing the charge on the gate-to-source capacitance C_{GS}. The gate power is frequency dependant and is determined by the following equation:

$$P_G = (Q_{GU} \bullet V_{GU} + Q_{GL} \bullet V_{GL}) \bullet F_S \quad \text{(EQ. 6)}$$

Q_{GU} = Upper MOSFET gate charge = 7.43nC

Q_{GL} = Lower MOSFET gate charge = 8.0nC

V_{GU} = Upper MOSFET gate voltage = 7V

V_{GL} = Lower MOSFET gate voltage = 12V

The gate drive power loss is:

$$P_G = (7.43 \bullet 10^{-9} \bullet 7 + 8.0 \bullet 10^{-9} \bullet 12) \bullet 400000 = 0.059\text{mW}$$

Switching Losses: The switching losses are caused by crossover conduction during the switching interval and by the output capacitance C_{OSS} being displaced. It turns out that the power dissipation caused by the output capacitance is very small compared to the conduction during switching and can be neglected. The switching losses become:

$$P_S = \frac{I \bullet V_{IN}}{2} \bullet t_{SW} \bullet F_S \quad \text{(EQ. 7)}$$

The switching transition t_{sw} takes place in approximately 10ns. Therefore:

Conduction Losses: Conduction losses are simply I^2R losses. Conduction losses can be approximated as:

$$P_S = \frac{7 \bullet 5}{2} \bullet 10^{-9} \bullet 400000 = 70\text{mW}$$

$$P_C = (R_{DSU} \bullet D + R_{DSL} \bullet (1 - D)) \bullet I^2 \quad \text{(EQ. 8)}$$

The HIP5011 data sheet $r_{DS(ON)}$ vs Temperature curve specifies that for a junction temperature of 110°C the value of $r_{DS(ON)}$ will increase by a factor of 1.45. Therefore:

$$R_{DSU} = 1.45 \bullet 0.039 = 0.057\Omega$$

$$R_{DSL} = 1.45 \bullet 0.041 = 0.060\Omega$$

$$P_C = (0.057 \bullet 0.727 + 0.060 \bullet (1 - 0.727)) \bullet 7^2 = 2.83\text{W} \quad \text{(EQ. 9)}$$

The total power loss of the SynchroFET at full load are:

$$P_T = P_G + P_S + P_C = 0.059 + 0.07 + 2.83 = 2.96\text{W}$$

This value matches very closely with the calculation of total power dissipated using empirical data shown earlier.

SynchroFET Operation With +5V Only

It is possible to “bootstrap” the SynchroFET off of a single +5V supply. To do this, five diodes and three capacitors are used to generate a charge-pump from the switching action of the converter. Using inexpensive 1N4148 diodes a V_{CC} of 11.5V can be achieved. Using Schottky diodes in place of the 1N4148’s, a V_{CC} in excess of 12V can be realize. The V_{CC} voltage can be created from the charge-pump technique shown in Figure 8.

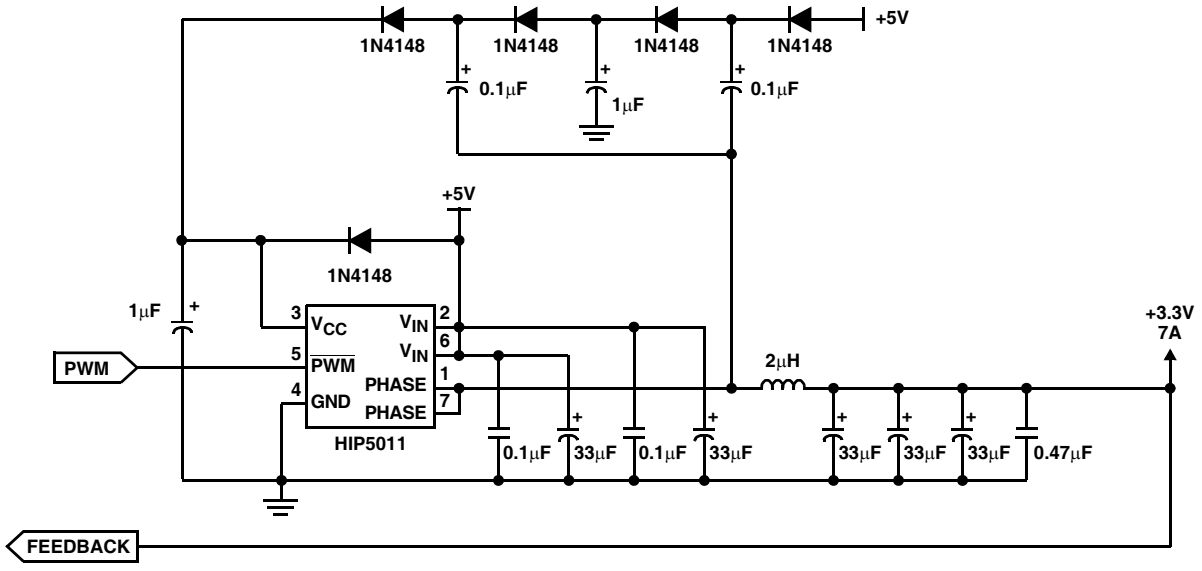

FIGURE 8.

The component selection of the charge pump circuit depends upon the switching frequency. The capacitors can be tantalum or ceramic, ceramic being the lowest cost. Each time charge is added to the capacitors (once every switching cycle) current flows in the diode and is limited by the diode's forward on resistance. The time constant of this resistance and the capacitor should be much less than the switching period. If using P-N junction diodes the designer should account for the reverse recovery losses when operating at very high frequencies (F_S > 500kHz). The SynchroFET will begin switching when V_{CC} is at least 4V. A diode from V_{IN} to V_{CC} will provide 4.3V to V_{CC}, satisfying the requirement for switching to begin.

Layout Considerations

While the SynchroFET is highly integrated and performs synchronous rectification transparent to the user, there is still just cause for proper layout. This is especially true if operation near or beyond 1MHz is planned. The critical areas for layout are supplying input power to the device, the phase connection and of course, ground. Figure 9 shows the component, solder, via and silk-screen layout of the HIP5011EVAL demo-board.

Since a typical bench supply will be used to evaluate the demo board performance, input bulk capacitors C2 and C3 decouple the input inductance from the +5V and +12V sources. In an actual embedded design, these may not be necessary.

High frequency input bypassing is performed by two pairs of capacitors C5, C8 and C6, C9. One pair for each V_{IN} terminal. Each pair of capacitors needs to be as close to the V_{IN} terminals as possible. They also need to have a short return path to ground. This arrangement will make a very tight high frequency bypassing path (see Figure 9).

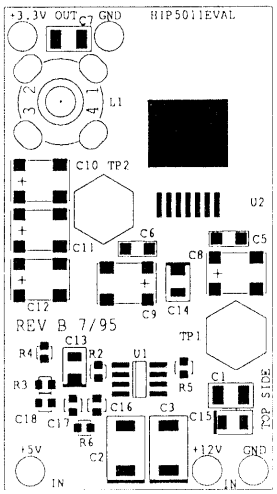

FIGURE 9A. SILK SCREEN

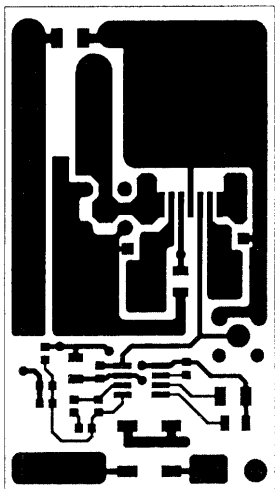

FIGURE 9B. COMPONENT SIDE

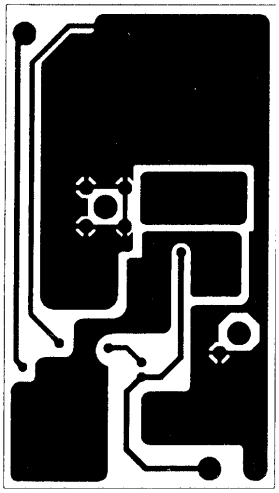

FIGURE 9C. SOLDER SIDE

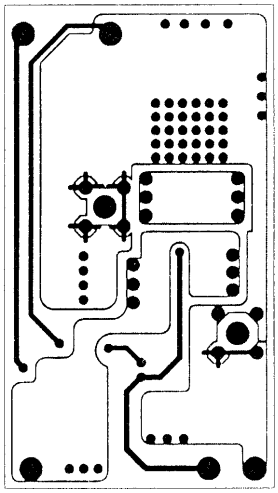

FIGURE 9D. SOLDER SIDE

The input and output capacitors should be tied to the same ground area. This ground area should be separate from the controller analog ground. The actual feedback path should consist of a separate ground and output power line from the output terminals to the controller signal ground and feedback terminal respectively.

The ground plane and input power plane should be as large as possible to eliminate parasitic inductances. A large ground plane will also aide thermal performance. Vias from the top side ground area, to the bottom side ground area, will transfer heat to a bottom side copper plane further improving thermal performance.

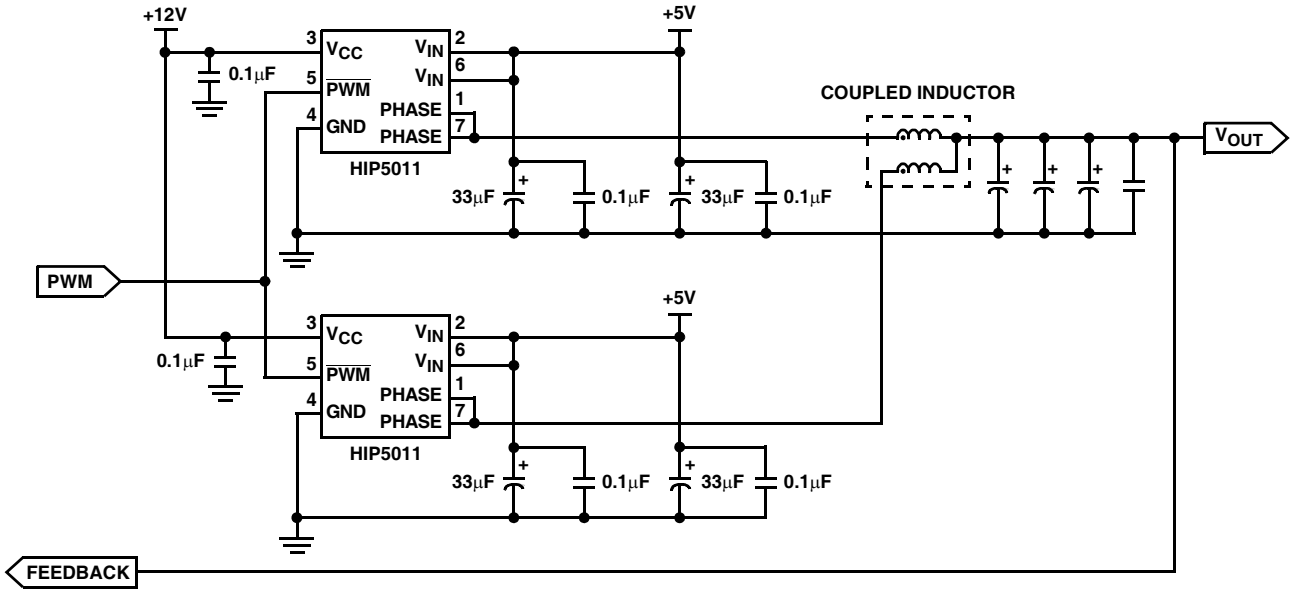

FIGURE 10.

Parallel Operation

Parallel operation of two SynchroFETs is possible for increased output current capability (an example of this is shown in Figure 10). In addition to following proper layout practices covered earlier there are several additional requirements for parallel operation.

- The PWM drive signal must have very fast rise and fall times because both SynchroFETs will not have the same input threshold.
- Both SynchroFETs must be grounded to the same continuous ground plane. This ensures that the PWM-to-ground voltage is the same for both packages.
- The printed circuit board routing of V_{CC}, V_{IN}, and PWM signal should be identical for both devices. This ensures the input inductance on the board will match to avoid delay mismatches.
- The two devices should have the identical thermal design. This ensures thermal tracking for each device and improves efficiency.

Performance

The performance of the HIP5011EVAL board proved to be excellent. Figure 11 shows the phase voltage along with the inductor current at no load. This shows the beauty of continuous conduction. At no load the inductor current traverses negative to maintain an average current of zero. Also, the phase voltage is absent of severe ringing as in discontinuous mode conduction.

The next two traces shown in Figures 12 and 13 are the inductor current under transient conditions. In Figure 12, the current is moving from no-load to full-load (7A). In Figure 13, the current moves from full-load to no-load. Again, notice the negative current which speeds up transient response.

Figure 14 shows a load transient di/dt moving from no-load to full-load, lasting 500µs and its effect on the output voltage. The output voltage remains in specification during this transient, for a total deviation of approximately 150mV.

In Figure 15 we have a short circuit condition. The short circuit current is shown in the top trace. The lower trace is the SCP control line, pin 5 on the TL5001. Its voltage increases to disable the PWM drive, which it does very nicely.

Shown in Figure 16 is the ripple voltage waveform at the full load current. The ripple voltage is quite higher than calculated. Possible reasons for this are additional contact resistance between the part and the board along with parasitic impedances.

Figure 17 shows the efficiency curve. From nearly 0.5A to over 5.5A the efficiency is 90% or greater and reaches 95% efficiency at 1.75A.

Finally, measurement on a network analyzer to determine actual loop response is shown in Figure 18. Here the unity gain crossover is at 60kHz with a phase margin of 75 degrees at full load. It was also measured at no load. At no load the crossover frequency was measured to be 40kHz and the phase margin was 50 degrees. As the load increases, the unity gain crossover increases because at higher current levels the inductance value of the output inductor decreases. This pushes the output filter pole pair further up the frequency scale.

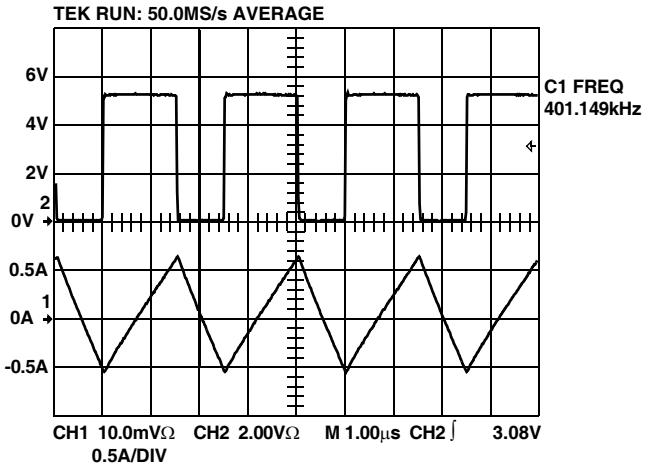

FIGURE 11.

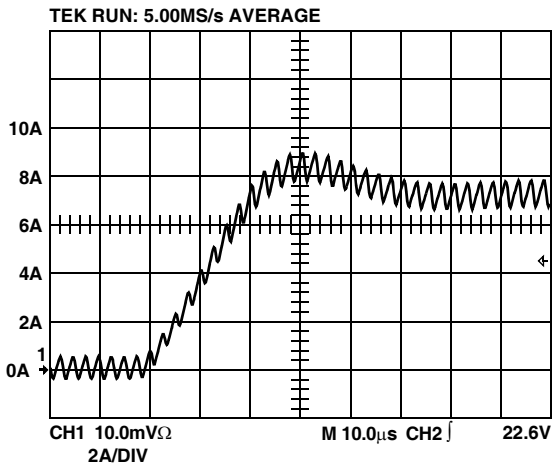

FIGURE 12.

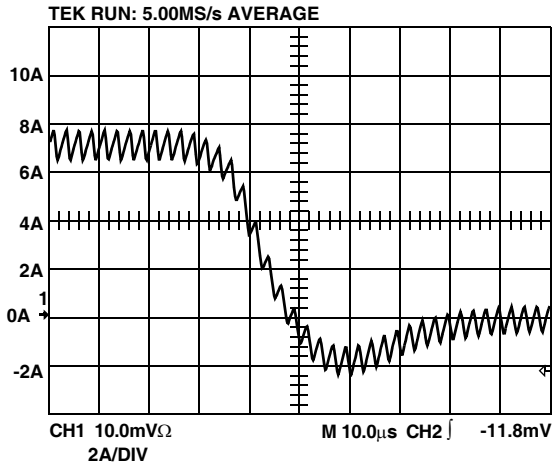

FIGURE 13.

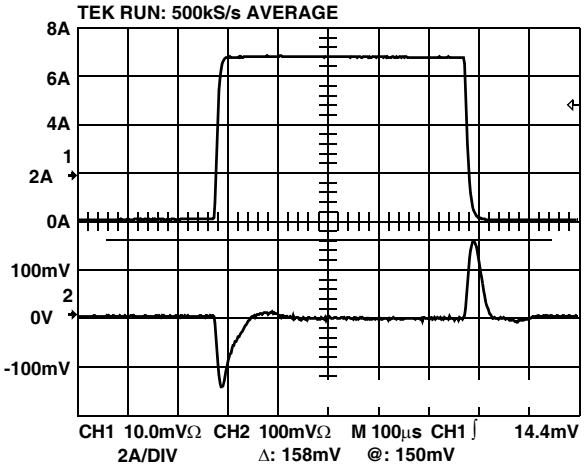

FIGURE 14.

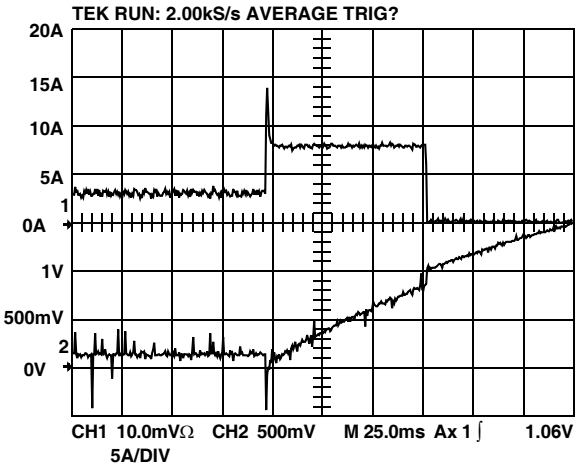

FIGURE 15.

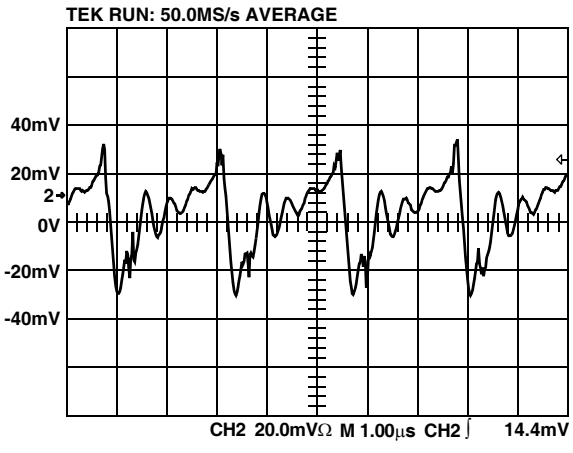

FIGURE 16.

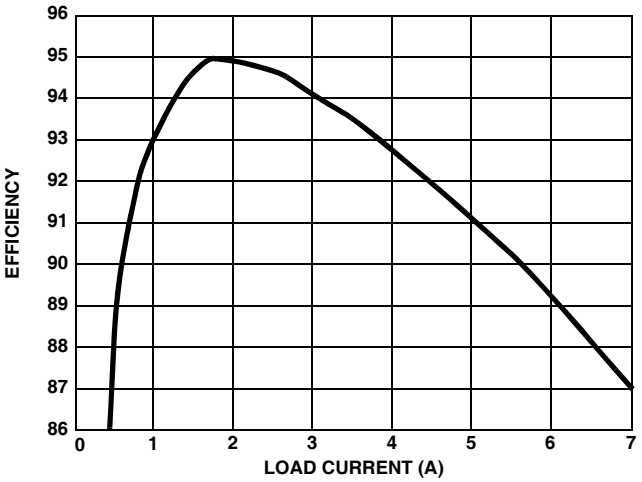

FIGURE 17. EFFICIENCY vs LOAD CURRENT

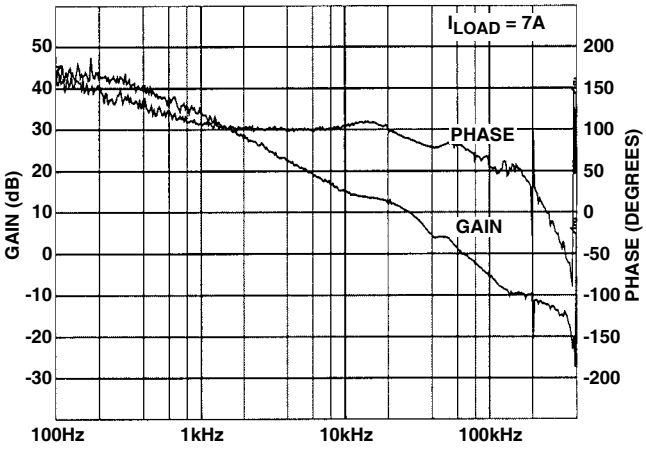

FIGURE 18.

Conclusion

The HIP5010 and HIP5011 SynchroFETs are a new approach in partitioning a synchronous rectified buck regulator. It has been demonstrated that a high performance synchronous rectified buck regulator can be realized using a very inexpensive controller. The SynchroFET facilitates the design of such a converter by integrating the control and power section into one device. Converters with output powers greater than 20W and efficiencies in excess of 90% can be easily implemented.

References

For Intersil documents available on the internet, see web site http://www.intersil.com.

[1] *HIP5010, HIP5011 Data Sheet*, Intersil Corporation, FN4029.

[2] Mike Walters, "*An Integrated Synchronous-Rectifier Power IC With Complementary-Switching*", Intersil Corporation, TechBrief No. TB332.

[3] *Designing With The TL5001C PWM Controller*, Texas Instruments Application Report #SLVA034.

[4] *TL5001C Data Sheet*, Texas Instruments, #SLVS084A.

[5] Abraham I. Pressman, *Switching Power Supply Design*, McGraw-Hill, 1991.

Material List

ITEM	QUANTITY	DESIGNATOR	VALUE
1	1	C1	0.22μF, 50V Ceramic
2	1	C2	100μF, 10V Tantalum
3	1	C3	4.7μF, 50V Tantalum
4	2	C5, C6	0.1μF, 50V Ceramic
5	5	C8, C9, C10, C11, C12	33μF, 6.3V Aluminum Polymer, Cornel Dubilier ESR330M0J1516
6	3	C13, C14, C15	1μF, 50V Tantalum
7	1	C7	0.47μF, 50V Ceramic
8	1	C16	390pF, 50V Ceramic
9	1	C17	5600pF, 50V Ceramic
10	1	C18	3900pF, 50V Ceramic
11	1	R2	3.32K, 1%
12	1	R3	3.4K, 1%
13	1	R4	1.47K, 1%
14	1	R5	15K, 1%
15	1	R6	2.43K, 1%
16	1	L1	2μH Inductor, CTX2-4 Coiltronics
17	2	TP1, TP2	Test-Point, Tektronix 131-4353-00
18	5	+5 IN, +12 IN, GND IN, 3.3V OUT, GND OUT	Terminal Post, Century Fasteners 1514-2
19	1	U1	TL5001C Texas Instruments
20	1	U2	HIP5011 Intersil Corporation